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PATENT NUMBER and  
ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10063737	05/09/2002	716	1	2825	Bowers

\*\*APPLICANTS: Hsu Jimmy;

\*\*CONTINUING DATA VERIFIED:

\*\* FOREIGN APPLICATIONS VERIFIED:

TAIWAN 91102057 02/06/2002

PG-PUB	DO NOT PUBLISH <input type="checkbox"/>	RESCIND <input type="checkbox"/>	
Foreign priority claimed 35 USC 119 conditions met Verified and Acknowledged Examiner's initials		<input checked="" type="checkbox"/> yes <input type="checkbox"/> no <input checked="" type="checkbox"/> yes <input type="checkbox"/> no BB	ATTORNEY DOCKET NO 8727-US-PA

TITLE : Voltage reference circuit layout inside multi-layered substrate

U.S. DEPT. OF COMM./PAT. & TM-PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G
Assistant Examiner		DRAWING	
		Sheets Drwg.	Figs. Drwg.
Primary Examiner		Print Fig.	
PREPARED FOR ISSUE		Application Examiner	
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